REMARKS

In the Office Action, claims 1 and 8-9 were rejected under 35 USC §103(a) as being unpatentable over Kobayashi et al. Claims 2 and 3 were rejected under 35 USC §103(a) as being unpatentable over Katti et al in view of Cernea et al. Claims 4-6 were rejected under 35 USC §103(a) as being unpatentable over Katti et al in view of Jaffe et al. Claim 7 was indicated to be allowable if rewritten in independent form.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

Concerning the claim rejection under 35 USC §103, the Examiner has rejected the claims as being unpatentable over U.S. Patent No. 4,811,294 (Kobayashi et al). This reference has not yet been formally made of record in the PTO-892. Correction is requested.

Firstly, it should be noted that the present invention concerns a sensing device for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors. In a general sense the present invention thus concerns sensing devices suitable for sensing a current response corresponding to a charge value, i.e. a polarization value of

ferroelectric memory cell wherein the polarization value is assigned as a binary 1 and a binary 0 according to some preselected protocol. In a passive memory cell of this kind of memory material proper, i.e. the ferroelectric material, always contacts the addressing electrodes, i.e., the word lines and the bit lines either in ohmic contact or capacitive contact. When data are written or read to a memory cell of this kind, leakage currents and noise also shall influence the polarization state of the other memory cells in the matrix, and for instance many non-addressed memory cells on the same bit line as the memory cell addressed for a read, influence the current signal output to the sense amplifier connected on this bit line.

Moreover, ferroelectric materials, particularly organic ones e.g. comprising a ferroelectric polymer, are subject to phenomena termed fatigue and imprint. Fatigue is the inherent tendency of a memory cell to lose some of its polarization or charge after write and read cycle, thus also reducing the signal/noise ratio after a large number of write and read cycles and making the detection less reliable. Imprint is a phenomenon manifest in the tendency shown by an unaddressed memory cell to be frozen in its initial polarization state, thus making it harder to effect either a read or write operation a time goes by. It should be noted that present-day technology relies on a so-called

destructive read such that the voltage potential applied over a memory cell between an active word line and an active bit line either leaves the memory cell in the same polarization state, outputting at most a weak current signal, or it will completely reverse the polarization state of the memory cell such that the write back must take place in order to reset the data initially written to the cell. As a consequence, in large passive matrix-addressable memories non-destructive readout may result in a polarization reversal and a large output current for approximately half of the memory cells of the memory matrix, assuming of course that logic ones and logic zeros are present in about equal numbers in suitably large memory. Thus a large current value is output in say half of the possible read operations and causes disturbances in the memory matrix, i.e. leakage currents, parasitic charges, disturb voltages etc., and the same of course will be the case when a reversed memory cell has to be reset by applying an equally large potential over the cell, but now of course with the opposite sign.

It is amply clear from the specification of the present application that it is a primary object to improve the resistance of the sensing device to noise and other interfering signals as mentioned in the introduction of the specification. As will be seen, also the read method as disclosed in the present application

appears particularly attractive with regard to handle fatigue and imprint in passive matrix-addressable ferroelectric memories.

The sensing device and the method according to the invention shall comport a considerable improvement over prior art, which in the present case must relate to passive matrix-addressable ferroelectric or electret memories which is precisely the devices that are hampered with the problems discussed above. Any examination that fails to take this into account will be misguided and lead to erroneous conclusions.

The Examiner relies on Katti et al. which is not concerned with ferroelectric memories at all, but rather with a memory based on magnetic memory cells wherein data are written and read magnetoresistively. A memory cell of this kind is addressed in an active mode and this means that the memory cells are connected with one or more switches so that outside any write and read cycle the former shall not be electrically connected with the addressing electrodes, i.e. the word lines and the bit lines of the memory matrix. Hence the problems encountered with passive matrix-addressable ferroelectric memory devices as set out above is not encountered in the memory device according to Katti et al. This is amply evident from the text, e.g. column 1, lines 40-54; "that allows data to be written to or read from the cell accurately *without interference* from surrounding cells "(emphasis added). Such

advantageous conditions of course will not be present in passive matrix-addressable memory devices as used with the present invention, and hence it, in contrast with Katti et al., aims at solving a completely different problem.

Of course one should as a matter of record be aware that sense amplifiers are commonly used in the detector circuits of matrix-addressable memories irrespective of whether they are based on either magneto-resistivity, ferroelectricity or optical phenomena, etc. The task set by the present invention is to obtain an accurate readout and a suitable sensing device for reading data in passive matrix memories, where the memory cells as stated above are ferroelectric capacitors and wherein of course the passive matrix memory is hampered by all the problems discussed hereinabove, problems which are clearly absent from the device as disclosed by Katti et al. As the Examiner observes, Katti et al discloses a voltage sense amplifier and this can be regarded as common prior art, but this of course does not make it obvious for a person of ordinary skill in the art how to solve the problems which are inherent and in particular to passive matrix-addressable ferroelectric memories.

The Examiner's statement (p.4) "that the voltage sense amplifier is functionally equivalent to the integrator circuit as claimed, of which is use (sic) for sensing current passing through

the memory cells" is correct, but not relevant in the present case where the problem is not sensing the current as such, but getting rid of noise and disturb components in the current so sensed. This problem is, however, not a matter of concern for Katti et al.

The Examiner rejects claims 2, 3 as unpatentable over Katti et al in view of Cernea et al (U.S. Patent No. 6,282,120). Cernea et al, however, concerns a transistor memory, i.e. floating gate memory such as EEPROM or flash EEPROM, and its stated object is to increase the storage capacity by providing memory cells suitable for multilevel coding, i.e. they can be written to more than two logic states. Further, Cernea et al., of course, provides for sensing circuitry able to perform the accurate readout when a multilevel coding is used. The memory cells of Cernea et al of course also are of the active type, i.e. the storage cell is switched for an addressing operation. Hence none of the problems encountered with passive matrix-addressable ferroelectric memories will be present in the memory device as disclosed by Cernea et al, and of course Cernea et al has no relevance for the problems the present invention aims to resolve. Finally, we observe that citing a non-relevant publication in view of another non-relevant publication shall not make the combination of the publications to by relevant or anticipatory to the present invention.

Concerning the rejection of claims 4-6 the Examiner again resorts to Katti et al, but admits the obvious difference between Katti et al and the present invention, and it is of no advantage combining Katti et al with U.S. patent No. 5,086,412 (Jaffe et al) which, although concerning a ferroelectric memory device, teaches this as an active matrix-addressable device, primarily of the 1T-1C type, i.e. with a switching transistor for each capacitive memory cell. Actually Jaffe et al show how to use a sample and hold circuit used for storing e.g. sensed current values to be compared for a read. More articularly, Jaffe et al which relies on said memory cells of the 1T-1C type, employs the fact that readout usually always are destructive, ie. there will be a polarization reversal of the memory cell dependent on the direction of the field applied, in other words on the sign of the voltage differential. To be specific, if positive polarization of a memory cell corresponds to a logic zero and a positive voltage difference is applied, the difference between a saturation polarization and the remanent polarization shall result in only a small current signal. Now storing this value and repeating the read, likewise a second small current signal will be obtained and a logic zero will be the output value. On the other hand, if the memory cell was in the opposite polarization state the positive voltage potential will result in a polarization reversal and a large output current is

detected. The polarization sense of these memory cells is of course reversed and it will drift from saturation back to the remanent polarization state. Now performing the second read with the same (positive) sign a small current signal will be output and the difference between the current values thus sensed will be large and a logic 1 can be assigned as the state of the memory cell. In this case of course a rewrite with a voltage of the opposite polarization must now take place in order to reset the original logic 1 stored in the memory cell thus read. However, this again does not take care of or solve the problems which were the sated object of the present invention and which of course will be inherent in all passive addressable ferroelectric memories as opposed to the active 1T-1C ferroelectric memory of Jaffe et al.

Concerning Fig. 7 of Katti et al it of course shows as stated the memory read electronics with a sense amplifier and a comparator, but for performing a non-destructive read. the function of the capacitor 714 in this case is to hold the current value which are used as a reference for providing a reference voltage V_n to the comparator. Then in a second phase of the read word current is switched to $+I_R$ and causes a resistance change in the selected memory cell 704 which is converted to a change in voltage by the sense current I_s and amplified in amplifier 700 to generate the read signal V_p at 706 which then is compared to the

reference level to determine the actual logic state of the cell, i.e. whether the binary 1 or 0 is stored. Hence, this arrangement of course does not address the problems that the present invention aims to solve and it is likewise seen that the disclosure in Jaffe et al which actually concerns ferroelectric active matrix-addressable ferroelectric memories will not be of much help either, it is just a matter of whether one must hold one or two current values, one of which of course shall be the reference. In Jaffe's case it will be required to store both the first and second sensed values, as it will be necessary to perform a reset in case the original data sorted in the cells is destroyed in the readout operation. This is of course, no issue with Katti et al which only concerns non-destructive readout in any case.

Since the prior art relied on by the Examiner concerns different types of active matrix-addressable memories or as is the case of Katti et al also a non-destructive read, the only thing shared by the present invention and the prior art cited is the use of a sense amplifier circuit. However, despite the apparent superficial similarity of e.g. the integrating comparator of Jaffe et al as shown in e.g. fig. 13a of the latter and the output stage with comparator in e.g. fig. 4 of the present application, there are apparent differences as the sensing device according to the present invention is devised to solve a problem fundamentally

different apart sensing from the logic states as such and this problem cannot be tackled by the sensing device according to Jaffe et al. Jaffe et al employs two read cycles for a detection, while the present invention relies on a "dual read", i.e. two consecutive reads in the same read cycle, the read values representing polarization differentials on the same polarization curve. By subtracting the second differential from the first, such that the error (noise) contributions appear as constant in the result, and then performing a threshold comparison. The logic state of the memory cell is reliably obtained even with heavily fatigued memory cells and high inherent S/N ratios in the differential values.

Based on the foregoing amendments and remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above amendments and remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

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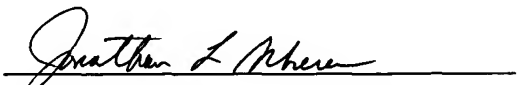
By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

Please amend the Abstract of the Disclosure as follows:

-- A sensing device ~~(10)~~ for reading data stored in a passive matrix memory ~~comprising~~ including memory cells in the form of ferroelectric capacitors, ~~comprises~~ includes an integrator circuit ~~(11)~~ for sensing the current response and ~~means (16, 17, 18)~~ a device for storing and comparing two consecutive read values, one of which is a reference value. In a read method for use with the sensing device a bit line is connected to the sensing device for sensing a charge flowing therebetween and a memory cell at the crossing of the former and activated word line, whereafter two consecutive reads of the memory cell are performed ~~an~~ and integrated over predetermined time periods in order to generate first and second read values which are compared for determining a logical value dependent on the sensed charge.

~~(Fig. 3)~~ --

IN THE CLAIMS:

Please cancel claims 7 without prejudice or disclaimer.

Please amend claims 1-6 as follows:

1. (Amended) A sensing device ~~(10)~~ for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors, wherein said sensing device ~~(10)~~ senses a current response corresponding to the data ~~, typically~~ including a binary one or a binary zero, and performs an integration of two read values, ~~characterized in that~~ the sensing device ~~(10)~~ comprises an integrator circuit ~~(11)~~ for sensing the current response and means ~~(16, 17, 18)~~ for storing and comparing two consecutive read values, one of which is a reference value.

2. (Amended) A sensing device~~(10)~~ according to claim 1, ~~characterized in that~~ wherein the integrator circuit ~~(1)~~ comprises an operational amplifier ~~(12)~~ and a capacitor ~~(C1)~~ connected between an inverting input ~~(14)~~ of the operational amplifier ~~(12)~~ and the output ~~(15)~~ thereof.

3. (Amended) A sensing device~~(10)~~ according to claim 2, ~~characterized in that~~ wherein the integrator circuit comprises a switch ~~(SW1)~~ connected in parallel over the capacitor ~~(C1)~~.

4. (Amended) A sensing device~~(10)~~ according to claim 1, ~~characterized in that~~ wherein the means ~~(16, 17, 18)~~ for two consecutive reads comprises a first sample/hold circuit ~~(16)~~ for sampling/storing a first read value, a second sample/hold circuit ~~(17)~~ for sampling/storing a second read value, and a comparator circuit ~~(18)~~ connected to the outputs of the sample/hold circuits ~~(16, 17)~~ for determining the state of an addressed memory cell.

5. (Amended) A sensing device~~(10)~~ according to claim 4, ~~characterized in that~~ wherein the sample/hold circuits ~~(16, 17)~~ comprise capacitors ~~(C_2, C^3)~~.

6. (Amended) A sensing device~~(10)~~ according to claim 4, ~~characterized in that~~ wherein the comparator circuit ~~(18)~~ is an operational amplifier.